REMARKS/ARGUMENTS

Interview Summary

During a telephone conversation with Examiner Phan on July 17, 2006, Applicants' representative suggested that the Final Office Action dated June 16, 2006, was premature because the rejection of the claims based on newly cited art included the rejection of claims 20, 21, 31, 32, 41 and 43 that were indicated as being allowable in the previous Office Action dated December 8, 2005; and that claims 20, 31 and 41 were amended in the Response to Office Action dated March 7, 2006, only to place them in independent form as requested by the Examiner.

The Examiner agreed and indicated that he would withdraw the Final Rejection. The Examiner stated that he has marked his file accordingly, and advised that this Response should be prepared as a Response to a non-final Office Action.

Remarks/Arguments

The Examiner has required that a new, more descriptive title be provided. The title of the application has been amended to read "**Method and System for Recording Events of an Interrupt Using Pre-Interrupt Handler and Post-Interrupt Handler**". Applicants believe this title is quite descriptive of the invention and is a proper title. If the Examiner believes the new title is still not satisfactory, it is respectfully requested that he suggest a suitable title.

Claims 1-53 are pending in the present application. No claims have been amended, added or canceled. Applicants have carefully considered the cited art and the Examiner's comments and believe the claims patentably distinguish over the cited art in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the following comments.

I. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 1-53 under 35 U.S.C. § 103(a) as being unpatentable over Hammond et al. (U.S. Patent No. 6,408,386 B1) in view of Henzinger et al. (U.S. Patent No. 5,857,097). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> In regard to claims 1, 12, 22, 33, 44, Hammond et al. disclose a method of processing performance information in a data processing system (see abstract), comprising the steps of: receiving an interrupt signal at an interrupt unit of a processor of the data processing system (see figure 5a&b, col. 9, line 57 through col. 10, line 48);

determining if at least one of a pre handler routine 233 and a post handler routine 243 are enabled for an interrupt (see figure 5a, col. 10, lines 29-49); invoking the pre handler routine to record events at a first instant if the pre handler routine is enabled (see col. 10, lines 36-42); invoking an interrupt handler routine following execution of the pre handler routine (see col. 10, lines 36-42); and invoking the post handler routine following execution of the post handler routine to record events at a second instant if the post handler routine is enabled (see col. 10, lines 42-48). But Hammond et al. do not specifically disclose the step of invoking an interrupt handler routines following execution of the interrupt handler routine to record events. However Henzinger et al. disclose the step of invoking an interrupt handler routines 1380 following the execution of the pre handler routine 1360 and invoking the post-handler routine 1390 following execution of the interrupt handler routine to record events (see figure 13, col. 23, line 48 through col. 24, line 30). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Henzinger et al. within the system of Hammond et al. because it would reduce the system stalled and improve the system performance.

Office Action dated June 16, 2006, pages 2-3.

Claim 1 of the present application is as follows:

1. A method of processing performance information in a data processing system, comprising the steps of:

receiving an interrupt signal at an interrupt unit of a processor of the data processing system;

determining if at least one of a pre handler routine and a post handler routine are enabled for an interrupt;

invoking the pre handler routine to record events at a first instant if the pre handler routine is enabled;

invoking an interrupt handler routine following execution of the pre handler routine; and

invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled.

Applicants respectfully submit that neither Hammond nor Henzinger nor their combination discloses or suggests "determining if at least one of a pre handler routine and a post handler routine are enabled for an interrupt", or "invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled" as recited in claim 1.

In rejecting the claims, the Examiner refers to Figure 5a and column 10, lines 29-49 of Hammond as disclosing "determining if at least one of a pre handler routine 233 and a post handler routine 243 are enabled for an interrupt". Column 10, lines 29-47 of Hammond is as follows:

When an exception generated by instruction set configuration **210** is received by event handling unit **233**, event handling unit **233** accesses a gate from interrupt descriptor table **410** as previously described. However, while in the configuration shown in FIG. **5a**,

> event handling unit **233** then inspects the accessed gate to determine whether it is a normal gate or an intercept gate. In one embodiment, this distinction is based on the state of an encoded bit field in the gate. A normal gate (e.g., gate **425**) contains the address of the exception's corresponding service routine (e.g., handler **400a**) according to the first system architecture. Upon accessing a normal gate, event handling unit **233** causes the processor to execute the handler identified by that gate (e.g., handler **400a**). In contrast, an intercept gate (e.g., intercept gate **435**) contains information identifying which event has occurred and that the event should be transferred to event handling unit **243**. Upon accessing an intercept gate, event handling unit **233** transfers event information (e.g., exception codes, vector numbers, etc.) to event handling unit **243**.

Nowhere in the above recitation is there any disclosure or suggestion that a determination is made whether either of event handling unit 233 or event handling unit 243 are enabled for an interrupt. The recitation simply describes what occurs when an exception generated by instruction set configuration 210 is received by event handling unit 233. A determination of whether or not components 233 or 243 are enabled is not disclosed. Therefore, even if event handling units 233 and 243 can be construed as pre and post handling units, Hammond still does not disclose or suggest "determining if at least one of a pre handler routine and a post handler routine are enabled for an interrupt" as required by claim 1.

Applicants also respectfully disagree that event handling unit 243 in Hammond can be construed as a post handler routine as suggested by the Examiner. The Examiner refers to column 10, lines 42-48, reproduced above as disclosing invoking a post handler routine. Applicants respectfully disagree. The recitation states only that intercept gate 435 contains information identifying which event has occurred and that the event should be transferred to event handling unit 243, and that upon accessing an intercept gate, event handling unit 233 transfers event information (e.g., exception codes, vector numbers, etc.) to event handling unit 243.

The recitation does not disclose invoking a post handler routine to record events at a second instant if the post handler routine is enabled as indicated by the Examiner. As described in col. 10, lines 29-47 of Hammond reproduced above, event handling unit 233 functions to determine whether exceptions should be forwarded to handlers 400a-i or to event handling unit 243 (Emphasis added). This is also made clear from the arrows in Figure 5a which point from event handling unit 233 to handlers 400a-i and from event handling unit 233 to event handling unit 243. Assuming *arguendo* that event handling unit 233 can be construed as a pre handler, event handling unit cannot be construed as a post handler routine that is invoked to record events at a second instant if the post handler routine is enabled. There is no arrow in Fig. 5a of Hammond that points from handlers 400a-i to event handling unit 243 which would be necessary, at the minimum, to attempt to construe unit 243 as a post handling unit.

In rejecting the claims, the Examiner acknowledges that Hammond does not specifically disclose the step of "invoking the post handler routine following execution of the interrupt handler routine to

record events at a second instant if the post handler routine is enabled" as recited in claim 1, but cites Henzinger as disclosing this feature. Specifically, the Examiner refers to component 1390 in Figure 13 of Henzinger as being a post handler routine that records events following execution of interrupt handler routines 1380.

Applicants respectfully disagree that Henzinger discloses a post handler routine of any kind, and that Henzinger discloses or suggests the step of "invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled" as recited in claim 1.

The Examiner refers to column 23, line 48 to column 24, line 30 of Henzinger, reproduced below, as teaching the post handler routine.

> During operation of the hardware, the fetch unit **1320** fetches instructions from the I-cache **1310** to queue up in the issue queue **1330**. Instructions are presented from the issue queue to the execution pipeline **1340**. In the preferred embodiment, multiple instructions can be issued during a single processor cycle. When an instruction successfully completes, the retire unit **1350** increments the retire counter **1360**. A program counter (pc) value associated with the retired instruction is stored in the IPR **1370**. The counter **1360** periodically generates an interrupt signal on line **1361**. In response, the interrupt handler **1380** can sample the counter **1360** and IPR **1370** to generate performance data **1390**. The sampled performance data will be substantial proportional to the number of times that an instruction at a particular program address (pc value) is retired.
>
> The number of "retire" events which are accumulated in the counter can be selected by presetting the counter to generate an interrupt on the overflow of a specific bit of the counter. The counter **1360** can be set by signals on set lines **1362**. An arbitrary interval between interrupts can be selected by setting the overflow bit position at the end of the interrupt handler. It is possible to choose intervals of random length. Alternatively, if the counter is implemented as a count-down register, the interval between interrupts can be selected by presetting the counter to a selected value. Here, the counter will interrupt on underflow, i.e., a zero value.
>
> In prior art implementations of performance counters, the interrupt handler generally has access to the program counter (pc) value of the next instruction to be executed when the interrupt handler completes; this pc value is sometimes called the "exception address," or the "return pc".
>
> However, simply recording this pc value does not accurately reflect the number of times the previous instruction was retired. In particular, if an instruction retires and the performance counter to overflows, the instruction has already been executed. In that case, the return pc does not reflect the pc value of the retired instruction.
>
> Depending on the details of interrupt processing, the return pc might be the instruction in the instruction stream immediately after the one whose retirement caused the interrupt, or it might be an variable number of instructions later, depending dynamically on the number of instructions in various stages of the fetch unit, issue queue, and execute pipeline.
>
> Therefore, if the interrupt handler **1380** simply records the return pc, then the sample counts recorded for each instruction using the "retire instruction" counter would not accurately reflect the execution frequency of the instructions.

As described above, component 1390 in Figure 13 of Henzinger is performance data generated by interrupt handler 1380. Specifically, Henzinger states: "the interrupt handler **1380** can sample the counter **1360** and IPR **1370** to generate performance data **1390**". This is not a disclosure of "invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled" as recited in claim 1. Performance data 1390 is data generated by the interrupt handler and is not a post handler routine that is invoked following execution of an interrupt handler routine to record events if the post handler routine is enabled Performance data 1390 would not appear to be a routine at all and is certainly not a post handler routine as recited in claim 1. Therefore, Henszinger also does not disclose or suggest "invoking the post handler routine following execution of the interrupt handler routine to record events at a second instant if the post handler routine is enabled"; and claim 1 patentably distinguishes over the references for this reason as well.

Yet further, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness in rejecting the claims as being unpatentable over Hammond in view of Henzinger. A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a rule exists that a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The requirements for establishing a *prima facie* case of obviousness in view of a combination of references are set forth in detail in Section 2142 of the MPEP and include the requirements that the Examiner explain in detail why the combination of the teachings is proper, that the Examiner provide a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of the references, and that the Examiner provide a showing that it is the prior art and not the Applicant's own disclosure that teaches the combination asserted by the Examiner.

Applicants respectfully submit that the Examiner has not set forth the basis of the rejection of claims 1-53 in sufficient detail to satisfy the requirements for establishing a *prima facie* case of obviousness with respect to the claims. Applicants respectfully submit that the Examiner has not provided a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of Hammond and Henzinger, and has not provided a showing

that it is the prior art and not the Applicants' own disclosure that has prompted the combination of Hammond and Henzinger asserted by the Examiner.

In particular, as discussed in detail above, neither Hammond nor Henzinger nor the combination of Hammond in view of Henzinger discloses or suggests a post handler routine. Only the present application discloses a post handler routine. Applicants believe, accordingly, that one of ordinary skill in the art, having Hammond and Henzinger before him would not find it obvious in view of the references to modify Hammond to provide a mechanism for invoking a post handler routine following execution of an interrupt handler routine to record events at a particular instant if the post handler routine is enabled; but instead, that it is Applicants' own disclosure that has prompted the combination of Hammond and Henzinger asserted by the Examiner. The Examiner's assertion that combining the references would reduce system stall and improve system performance is not a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of Hammond and Henzinger. The Examiner, therefore, has not established a *prima facie* case of obviousness in rejecting the claims, and claim 1 is also not unpatentable over the references for this reason as well.

For at least all the above reasons, claim 1 patentably distinguishes over the references in its present form, and it is respectfully requested that the Examiner so find.

Independent claims 12, 20, 22, 31, 33, 41 and 44 are also not obvious over Hammond in view of Henzinger for similar reasons as discussed above with respect to claim 1. Claims 2-11, 13-19, 21, 23-30, 32, 34-40, 42-43 and 45-53 depend from and further restrict one of the independent claims and are also not unpatentable over Hammond in view of Henzinger, at least by virtue of their dependency. In addition, many of these claims recite additional features which are not disclosed or suggested by the references such that the claims patentably distinguish over the references in their own right as well as by virtue of their dependency. For example, inasmuch as the references do not disclose a post handler routine, the references also do not disclose or suggest "a plurality of pre handler routines and a plurality of post handler routines, wherein each pre handler routine and each post handler routine records a different event on the occurrence of an interrupt" as recited in claims 7, 18, 28, 39 and 51.

Therefore, the rejection of claims 1-53 under 35 U.S.C. § 103 has been overcome.

II. Conclusion

For all the above reasons, it is respectfully urged that claims 1-53 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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